07-03-00

Please type a plus sign (+) inside this box → +

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office U S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P8527
First Inventor or Application Identifier	Brad A. Barmore
Title	MOTHERBOARD EXTENSION FEATURES TO PROVIDE ...
Express Mail Label No.	EL034434111US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [Total Pages 19]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [Total Sheets 7]

4. Oath or Declaration [Total Pages 4]
a. ☒ Newly executed (original copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☒ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☒ Other: Check for $856.00

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

16. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:

Prior application Information: Examiner _____ *Group/Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or ☒ *Correspondence address below*

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	State	California	Zip Code	90025
Country	U.S.A.	Telephone	(503) 684-6200	Fax	(503) 684-3245

Name (Print/Type)	Paul A. Mendonsa, Reg. No. 42,879		
Signature	Paul A. Mendonsa	Date	06/30/00

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

042390.P8527 *Patent*

UNITED STATES PATENT APPLICATION

FOR

MOTHERBOARD EXTENSION FEATURES TO PROVIDE PLUG AND PLAY INFORMATION

INVENTOR:

BRAD A. BARMORE

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026

(503) 684-6200

EXPRESS MAIL NO. EL 034434111 US

MOTHERBOARD EXTENSION FEATURES TO PROVIDE PLUG AND PLAY INFORMATION

FIELD OF THE INVENTION

The invention relates to electronic systems, such as computer systems, thin clients, or set top boxes. More particularly, the invention relates to riser cards providing electronic system motherboard feature extension with plug and play functionality.

BACKGROUND OF THE INVENTION

Electronic system motherboards are becoming increasingly integrated to support a growing number of features and/or more compact packaging. The motherboard is the physical arrangement that contains the system's basic circuitry and components. Typically, motherboards have circuitry imprinted or affixed to the surface of a printed circuit board (PCB) or other similar component. Motherboards commonly include the microprocessor, co-processors (if any), memory, basic input/output system (BIOS), expansion slots, and interconnecting circuitry. Additional components can be coupled to a motherboard through its expansion slots. Common expansion slot standards are the Peripheral Component Interconnect (PCI) standards available from the PCI Special Interest Group of Portland, Oregon.

However, motherboard integration of features traditionally included in common expansion slots has been problematic for several reasons including Federal Communications Commission (FCC) and international telecommunications certification, motherboard space and other manufacturer specific requirements. FCC and international telecommunications certifications require, for example, that an electronic system not

interfere in frequency ranges reserved for other uses (e.g., 900 MHz telephones).

Increased integration is performed to decrease the overall cost of the computer system.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a block diagram of one embodiment of an electronic system.

Figure 2 illustrates one embodiment of a Communications and Networking Riser (CNR) and associated slot.

Figure 3 illustrates a block diagram of one embodiment of a CNR interface.

Figure 4 illustrates one embodiment of a CNR providing an analog modem with a phone line network interface, in an electronic system containing an audio codec.

Figure 5 illustrates one embodiment of a CNR providing an audio-down codec with a 10/100 LAN interface in an electronic system containing an audio codec.

Figure 6 illustrates one embodiment of a CNR providing audio and modem codecs and a phone line networking interface.

Figure 7 illustrates one embodiment of a CNR providing an audio/modem codec and a phone line networking interface.

Figure 8 illustrates one embodiment of a CNR providing a multi-channel audio upgrade to an electronic system containing an audio codec.

Figure 9 is a conceptual illustration of a SMBus configuration for use with a riser card and multiple memory devices.

DETAILED DESCRIPTION

Methods and apparatuses for motherboard and riser card Plug-and-Play (PnP) functionality support are described. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

A riser card is an extension of the motherboard to which it is attached. Logically, the riser card is a portion of the motherboard. Physically, the riser card is attached to the motherboard through a connector or other type of interface, and can be more easily removed and replaced than typical motherboard-mounted components. Thus, like motherboard mounted components, the functionality of the riser card is typically determined during boot up of the system.

A riser card with a corresponding interface on a motherboard can reduce the overall cost of an electronic system as well as simplify upgrading the features provided by the electronic system. Implementation costs can be reduced, for example, for sensitive analog components that may otherwise require shielding in order to prevent

electromagnetic interference if the same analog components were located on the motherboard. Other components can also be simplified if located on a riser rather than the motherboard. Upgrading of features supported by the electronic system is simplified because the riser card can be installed or replaced to enhance the existing features of the electronic system. The riser card described herein provides PnP functionality so that an operating system controlling the electronic system in which the riser card is included can load the appropriate driver software thereby simplifying operation of the electronic system.

Figure 1 is a block diagram of one embodiment of an electronic system. The system illustrated in Figure 1 is intended to represent a range of electronic systems including, but not limited to, computer systems, set top boxes and thin clients. Alternative systems can include more, fewer and/or different components.

System 100 includes bus 101 or other communication device to communicate information, and processor 102 coupled to bus 101 to process information. While system 100 is illustrated with a single processor, system 100 can include multiple processors and/or co-processors. System 100 further includes random access memory (RAM) or other dynamic storage device 104 (referred to as main memory), coupled to bus 101 to store information and instructions to be executed by processor 102. Main memory 104 also can be used to store temporary variables or other intermediate information during execution of instructions by processor 102.

System 100 also includes read only memory (ROM) and/or other static storage device 106 coupled to bus 101 to store static information and instructions for processor 102. Data storage device 107 is coupled to bus 101 to store information and instructions.

Data storage device 107 such as a magnetic disk or optical disc and corresponding drive can be coupled to system 100.

System 100 can also be coupled via bus 101 to display device 121, such as a cathode ray tube (CRT) or liquid crystal display (LCD), to display information to a computer user. Alphanumeric input device 122, including alphanumeric and other keys, is typically coupled to bus 101 to communicate information and command selections to processor 102. Another type of user input device is cursor control 123, such as a mouse, a trackball, or cursor direction keys to communicate direction information and command selections to processor 102 and to control cursor movement on display 121.

System 100 further includes Communication and Network Riser (CNR) 130 to provide access to a network, such as a local area network, as well as provide communications functionality, such as audio input/output, Local Area Network (LAN) or a modem connection. As described herein, CNR 130 is used as an exemplary riser card. Other types of riser cards providing other types of functionality can be similarly supported. In one embodiment, CNR 130 physically separates noise sensitive systems from the noisy environment of the motherboard. Placing the communications and networking components on CNR 130 also simplifies motherboard design and provides easier upgrade of communications and networking components.

As described in greater detail below, CNR 130 provides PnP functionality. In one embodiment, CNR 130 includes an Electrically Erasable Programmable Read only Memory (EEPROM) or other memory device (not shown in Figure 1) that provides sufficient information related to the functionality of CNR 130 that a Basic Input/Output System (BIOS), operating system, or other service can load the appropriate drivers to

support the functionality of the CNR 130. In one embodiment, the BIOS, operating system, or other service is represented as a sequence of instructions in a machine-readable medium.

As used herein, a machine-readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals), etc.

Figure 2 illustrates one embodiment of a Communications and Networking Riser (CNR) and associated slot. In one embodiment, motherboard 200 includes multiple expansion slots 220 as well as a CNR slot 215 to receive a CNR card 130. In one embodiment, expansion slots 220 are Peripheral Component Interconnect (PCI) expansion slots. In alternate embodiments, other types of expansion slots can be provided. Use of such industry standard expansion slots is well known in the art. In alternate embodiments other types of risers or motherboard extensions can be provided.

In general, a riser card is a logical extension of the motherboard. In other words, the riser card operates as if it were a part of, or coupled to, the motherboard. In contrast, expansion card, such as PCI expansion cards, operate independent of the motherboard.

In one embodiment, slot 215 is also coupled to motherboard 200. In Figure 2, slot 215 is illustrated as a female connector; however, slot 215 can be implemented as a male connector. CNR 130 is configured to connect to slot 215. CNR 130 includes hardware components for use with the components of motherboard 200. For example, CNR 130

can include modem hardware, audio codec hardware, network interface hardware, etc. One or more of the hardware components of CNR 130 has a corresponding software driver that is executed by a processor on motherboard 200.

Identification and loading of the proper software drivers is described in greater detail below. In one embodiment, CNR 130 supports multi-channel audio, V.90 analog modem, phone-line based networking and/or 10/100 Ethernet based networking. In alternate embodiments, CNR 130 supports additional and/or different services (e.g., wireless networking, video, other modem protocols, etc.).

Figure 3 illustrates a block diagram of one embodiment of a Communication and Networking Riser (CNR) interface. The block diagram of Figure 3 illustrates several specific interfaces; however, any number or types of interfaces can be supported. Thus, the description with respect to Figure 3 is for explanation purposes and should not be read as limiting as to the interfaces that can be provided between a riser card and a motherboard.

The specific interfaces illustrated in Figure 2 are Audio Codec '97 (AC '97), one or more network interfaces (LAN interfaces), a Universal Serial Bus (USB) interface, a System Management Bus (SMBus) interface, power lines and a set of reserved lines. In alternate embodiments, other interfaces can be provided.

AC '97 is described in Audio Codec '97 Component Specification, Revision 2.1 published May 22, 1998 by Intel Corporation. In one embodiment, two AC '97 codecs are supported; however, any number of AC '97-compliant codecs can be supported. LAN interfaces generally refers to a set of signals to communicate via a network according to an appropriate protocol. USB is described in Universal Serial Bus

Specification, Revision 1.1, published the USB Implementer's Forum (USB-IF) of Portland, Oregon. The System Management Bus Version 1.1 interface specification is available from Intel Corporation of Santa Clara, California.

Figure 4 illustrates one embodiment of a CNR providing an audio-down codec, modem codec, and a phone line network interface. In the embodiment, the AC '97 primary codec down 400 is located on the motherboard and is coupled with CNR 130 via the AC '97 portion of interface 310. CNR 130 includes a MC '97 secondary codec up coupled with the AC '97 portion of interface 310. A Data Access Arrangement (DAA) 420 is coupled to codec 410. DAA 420 is an electronic interface between codec 410 and a public telephone line via RJ-11 jack 450. A DAA is also sometimes called a Telephone Line Interface Circuit (or Module). DAAs are typically required in any device that attaches to the public switched telephone network (PSTN), including fax machines, PBXs, set-top boxes, and alarm systems. Among other things, DAA 420 isolates the electronic device from the higher voltage on the telephone line.

Phone-line PLC/PHY up 430 and network interface/isolation circuit 440 is also coupled between the LAN interface portion of 310 and RJ-11 jack 450 to provide a networking interface. Other components (e.g., USB components, EEPROM or other memory), which are not shown for reasons of simplicity of description, can also be included on CNR 130.

Figure 5 illustrates one embodiment of a CNR providing an audio-down codec with a 10/100 LAN interface. CNR 130, as illustrated in Figure 5, supports Ethernet-based networking with 10/100 LAN PLC/PHY up 500, network interface/isolation 510

and RJ-45 jack 520. In one embodiment, CNR 130 also includes the codecs and other components described above.

Figure 6 illustrates one embodiment of a CNR providing audio and modem codecs and a phone line networking interface. CNR 130, as illustrated in Figure 6, supports phone line networking as described above. CNR 130 also includes audio support circuitry 600 and audio I/O interface 610 to provide audio functionality. Other components can also be included on CNR 130.

Figure 7 illustrates one embodiment of a CNR providing an audio/modem codec and a phone line networking interface. Figure 7 illustrates an alternative embodiment having audio/modem support and phone line networking. Other components can also be included on CNR 130.

Figure 8 illustrates one embodiment of a CNR providing a multi-channel audio upgrade. Figure 8 illustrates CNR 130 with AC '97 secondary codec up 800, audio amplifier 810 and audio output jacks 820 to support multi-channel audio. Other components can also be included on CNR 130.

Figures 4-8 illustrate situations in which use of a CNR can reduce manufacturing costs. The desired communication and networking solution can be provided by inserting the CNR with the desired functionality without redesign of the motherboard.

In one embodiment, a system implementing an architecture with CNR 130 functionally treats CNR 130 as an extension of motherboard 200. This implies that the BIOS identifies the functionality provided by CNR 130 and implements appropriate support to provide properly configured interfaces. Operating systems have improved in the ability to use standardized registers to uniquely identify hardware added to a system

and to provide the appropriate drivers for the hardware. In one embodiment, CNR 130 provides a Plug-and-Play (PnP) type interface.

In one embodiment, the PnP interface includes registers for Vendor ID (VID), Device ID (DID), Subsystem Vendor ID (SVID) and Subsystem ID (SID). Interfaces using other registers and/or identifiers can also be used. Because the front end (either digital or analog) functionality can be provided by different suppliers, with each implementing the surrounding support circuitry in a different manner, the identifiers associated with the functionality of CNR 130 are provided by some component of CNR 130.

In one embodiment PnP information related to CNR 130 is provided to an operating system using a combination of a SMBus based EEPROM and specialized BIOS routines. The electrical interface to the EEPROM is provided on the CNR connector through the signals SMB_SCL, SMB_SDA, SMB_A2, SMB_A1 and SMB_A0, each of which are defined by the SMBus standard. In alternate embodiments, other signals and/or interfaces can be used to provide the PnP information.

In one embodiment, the EEPROM is byte addressable and is SMBus address configurable through external strapping for use on an SMBus that may contain one or more memory devices. Other types of memories can also be used to provide PnP information as described herein.

Figure 9 is a conceptual illustration of one embodiment of a SMBus configuration for use with a riser card and multiple memory devices. Figure 9 illustrates one embodiment in which memory banks 910 and 920 and EEPROM 950 have unique addresses, which are 001b, 000b and 100b, respectively. SMBus controller 900

communicates with, and controls, memory banks 910 and 920 and EEPROM 950 over SMBus 970. Use and configuration of SMBus 970 and SMBus controller 900 are known in the art.

In one embodiment, EEPROM 950 includes a master configuration space that is used by sequences of instructions stored in BIOS 990 that, when executed, determine the functionality supported by CNR 130. The master configuration space can also be used to determine where, within EEPROM 950, information related to each functionality is located along with the amount of memory each function uses. In one embodiment, instructions within BIOS 990 cause the associated electronic system to determine the functions supported by CNR 130, properly detect front end associated with each function, extract the information within EEPROM 950 associated with each function, and place the extracted data within the registers associated with each function.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A system comprising:

a motherboard to have a chipset coupled thereto;

a memory to store a sequence of instructions, the memory coupled with the motherboard; and

a riser card coupled with the motherboard, the riser card having a circuit thereon that interacts with a corresponding portion of the chipset to provide a functionality to the system, the riser card also having a memory to store one or more indications of the functionality;

the sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications.

2. The system of claim 1 wherein the riser card is coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined industry standards.

3. The system of claim 1 wherein the memory of the riser card is a read-only memory (ROM) and the boot sequence is a basic input/output system (BIOS).

4. The system of claim 1 wherein the functionality comprises one or more audio codecs.

5. The system of claim 1 wherein the functionality comprises one or more modem codecs.

6. The system of claim 1 wherein the functionality comprises support for one or more Universal Serial Bus devices.

7. The system of claim 1 wherein the functionality comprises support for one or more SMBus devices.

8. The system of claim 1 wherein the functionality comprises networking functionality.

9. The system of claim 1 wherein the driver is loaded by an operating system.

10. A riser card comprising:

a interface to allow the riser card to be coupled with a motherboard having a chipset coupled thereto;

a memory to store a sequence of instructions, the memory coupled with the motherboard; and

a riser card coupled with the motherboard, the riser card having a circuit thereon that interacts with a corresponding portion of the chipset to provide a functionality to the

system, the riser card also having a memory to store one or more indications of the functionality;

the sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications.

11. The card of claim 10 wherein the riser card is coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined industry standards.

12. The card of claim 10 wherein the memory on the riser card is a read-only memory (ROM) and the boot sequence is a basic input/output system (BIOS).

13. The card of claim 10 wherein the functionality comprises one or more audio codecs.

14. The card of claim 10 wherein the functionality comprises one or more modem codecs.

15. The card of claim 10 wherein the functionality comprises support for one or more Universal Serial Bus devices.

16. The method of claim 10 wherein the functionality comprises support for one or more SMBus devices.

17. The card of claim 10 wherein the functionality comprises networking functionality.

18. The card of claim 10 wherein the driver is loaded by an operating system.

19. A memory comprising an interface to couple to a riser card, the riser card having a circuit thereon that interacts with a corresponding portion of the chipset to provide a functionality to the system, the memory to store one or more indications of the functionality.

20. The memory of claim 19 wherein the riser card is coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined industry standards.

21. The card of claim 19 wherein the memory is a read-only memory (ROM).

22. The card of claim 19 wherein the functionality comprises one or more audio codecs.

23. The card of claim 19 wherein the functionality comprises one or more modem codecs.

24. The card of claim 19 wherein the functionality comprises support for one or more Universal Serial Bus devices.

25. The card of claim 19 wherein the functionality comprises support for one or more SMBus devices.

26. The card of claim 19 wherein the functionality comprises networking functionality.

27. The card of claim 19 wherein the driver is loaded by an operating system.

ABSTRACT

A riser card with a corresponding interface on a motherboard can reduce the overall cost of an electronic system as well as simplify upgrading the features provided by the riser. Implementation costs can be reduced, for example, for audio components that may otherwise require shielding in order to prevent electromagnetic interference if the audio component were located on the motherboard. Other components can also be simplified if located on a riser rather than the motherboard. Upgrading of features supported by the riser card is simplified because the riser card can be replaced. The riser card described herein provides Plug-and-Play functionality so that an operating system controlling the electronic system in which the riser card is included can load the appropriate driver software thereby simplifying operation of the electronic system.

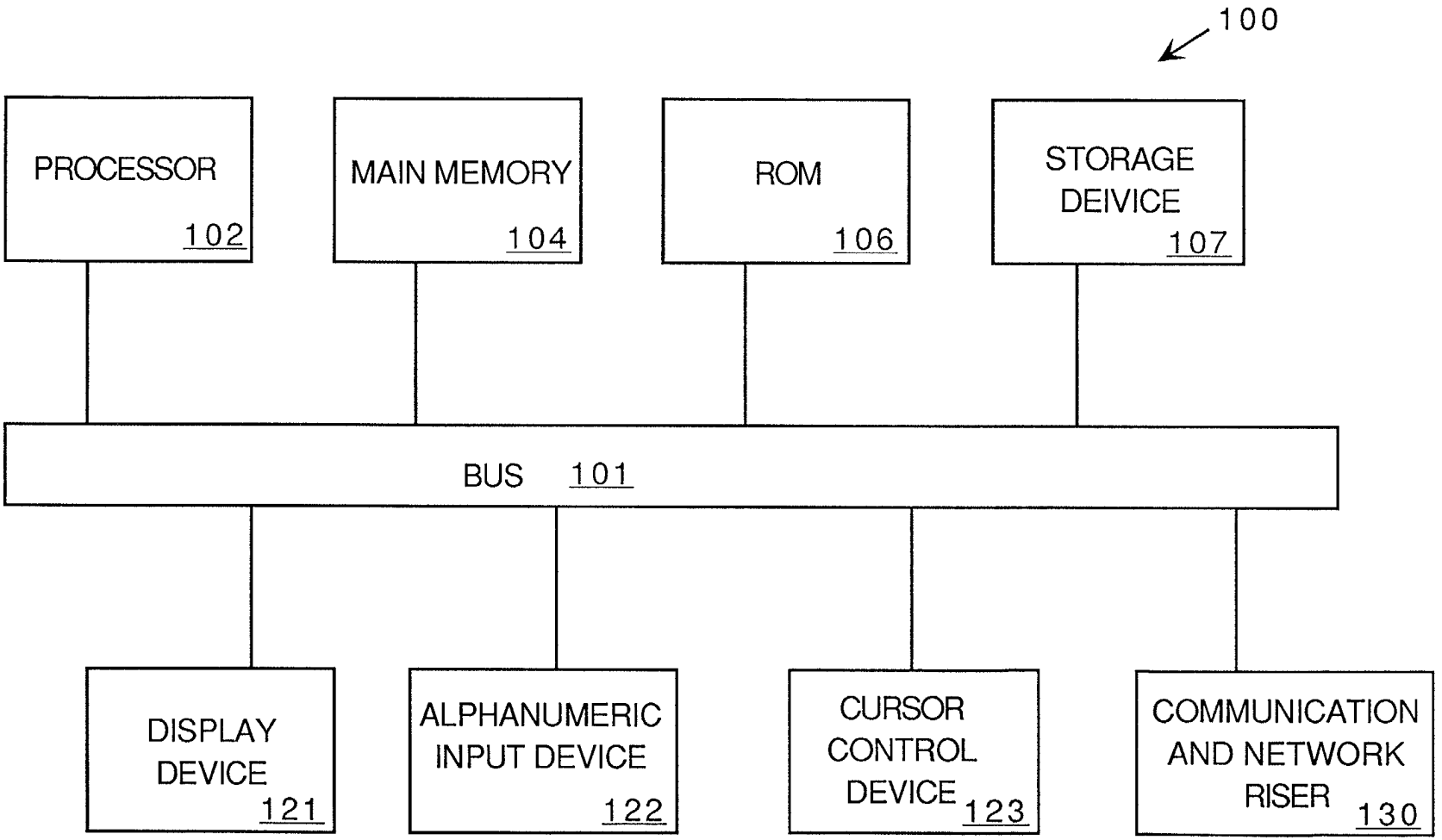
100
PROCESSOR
102
MAIN MEMORY
104
ROM
106
STORAGE
DEIVICE
107
BUS 101
DISPLAY
DEVICE
121
ALPHANUMERIC
INPUT DEVICE
122
CURSOR
CONTROL
DEVICE 123
COMMUNICATION
AND NETWORK
RISER 130

FIG. 1

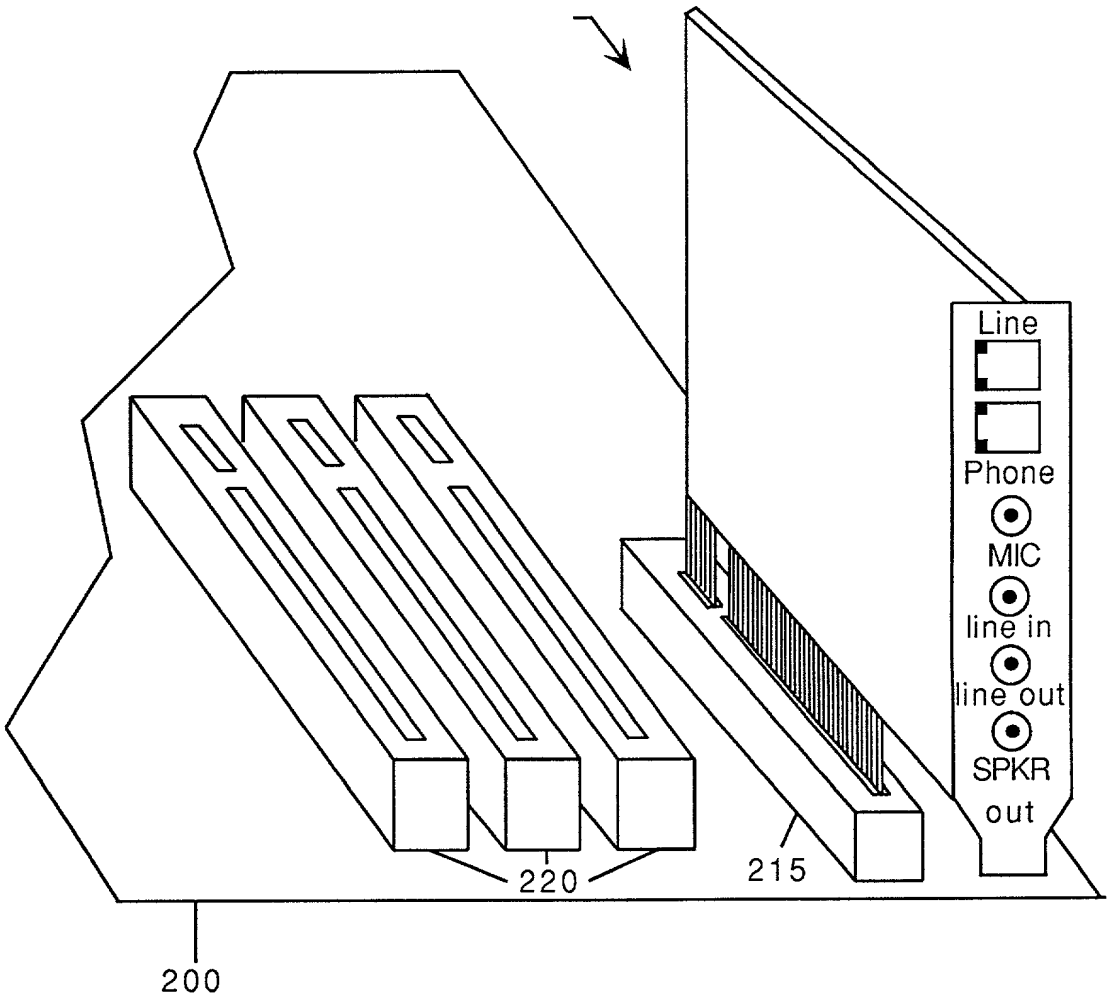

FIG. 2

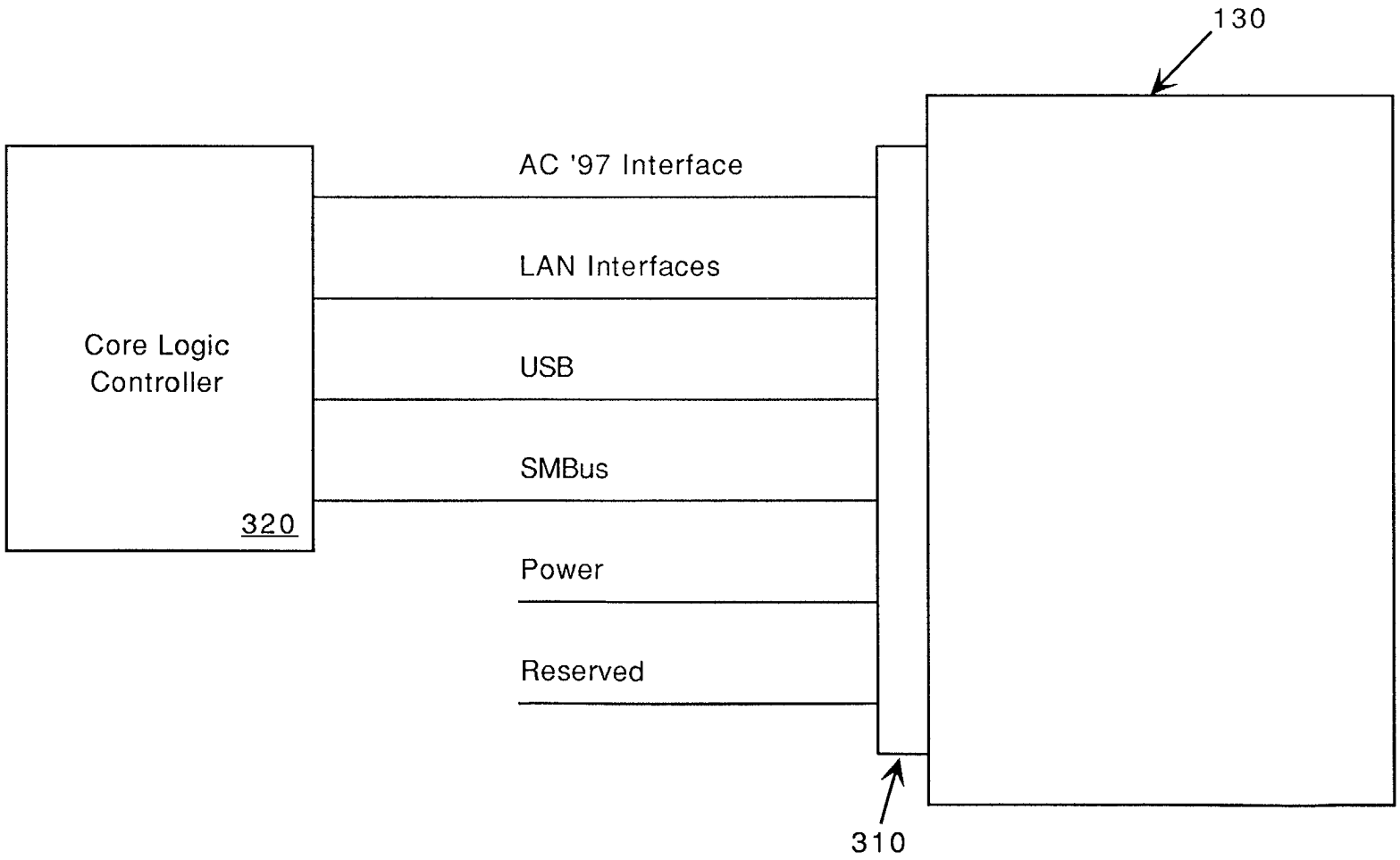
130
AC '97 Interface
LAN Interfaces
USB
SMBus
Power
Reserved
Core Logic
Controller
320
310

FIG. 3

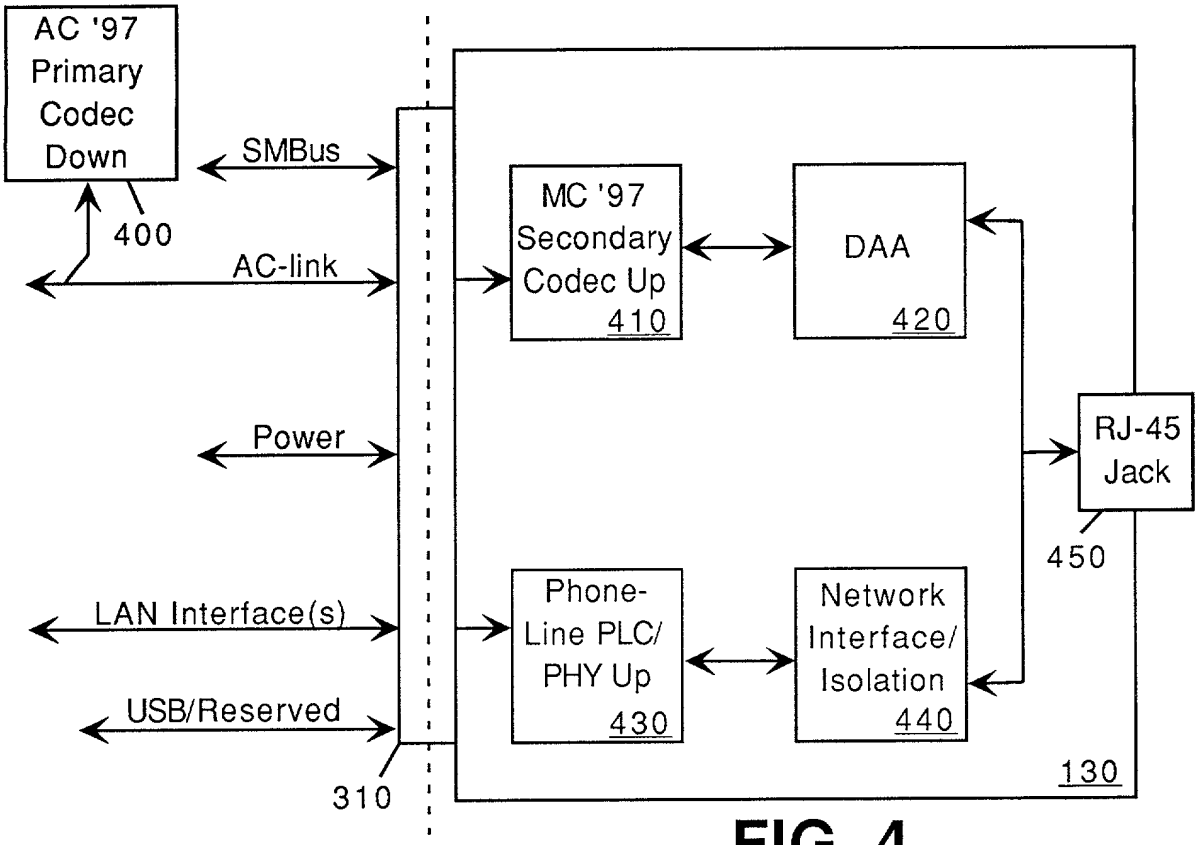
AC '97
Primary
Codec
Down
SMBus
400
AC-link
Power
LAN Interface(s)
USB/Reserved
310
MC '97
Secondary
Codec Up
410
DAA
420
RJ-45
Jack
450
Phone-
Line PLC/
PHY Up
430
Network
Interface/
Isolation
440
130

FIG. 4

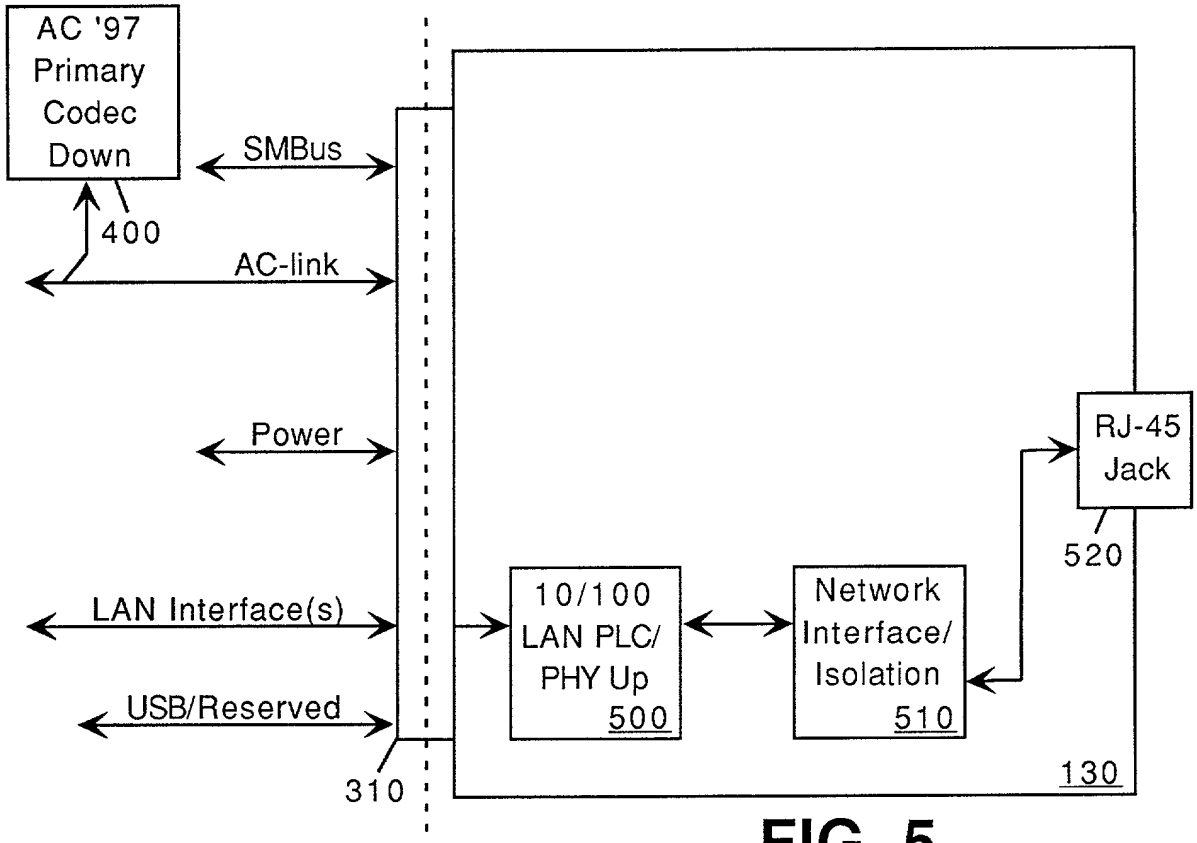
AC '97
Primary
Codec
Down
SMBus
400
AC-link
Power
LAN Interface(s)
USB/Reserved
310
10/100
LAN PLC/
PHY Up
500
Network
Interface/
Isolation
510
RJ-45
Jack
520
130

FIG. 5

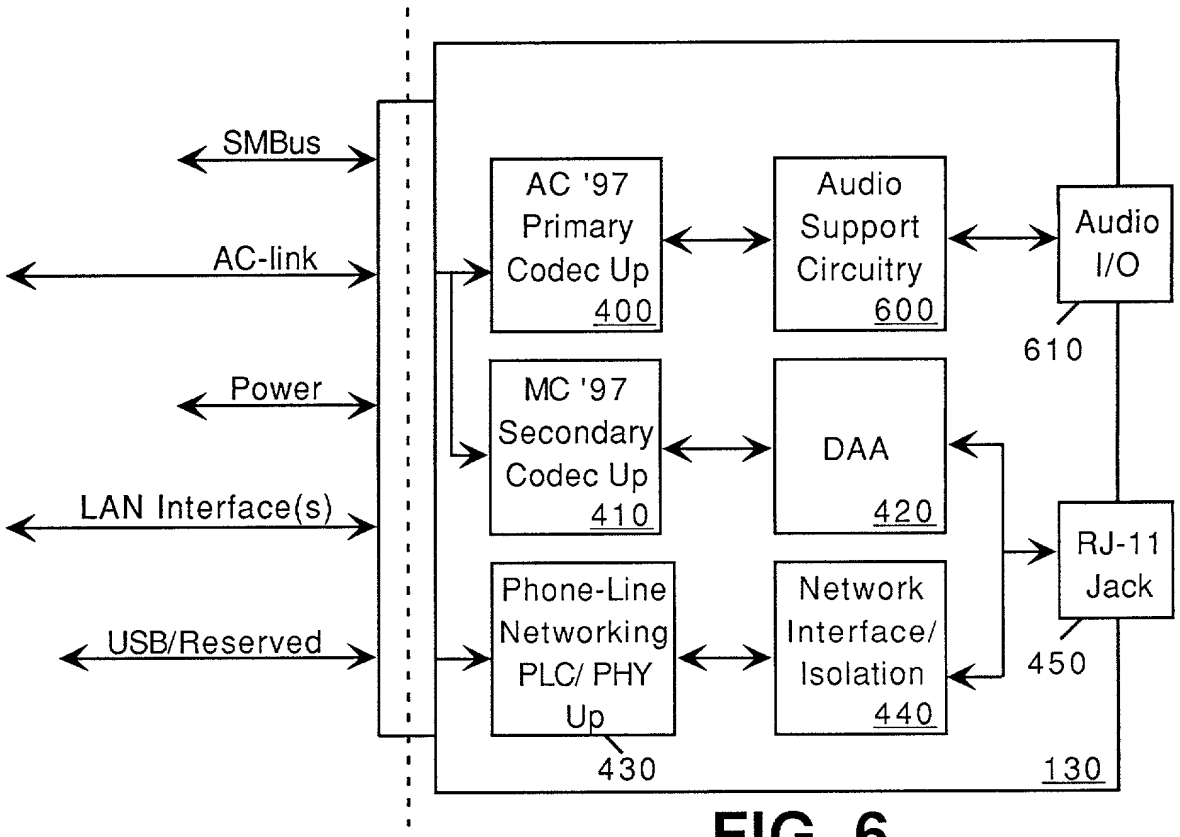
SMBus
AC-link
Power
LAN Interface(s)
USB/Reserved
AC '97 Primary Codec Up 400
MC '97 Secondary Codec Up 410
Phone-Line Networking PLC/ PHY Up 430
Audio Support Circuitry 600
DAA 420
Network Interface/ Isolation 440
Audio I/O 610
RJ-11 Jack 450
130

FIG. 6

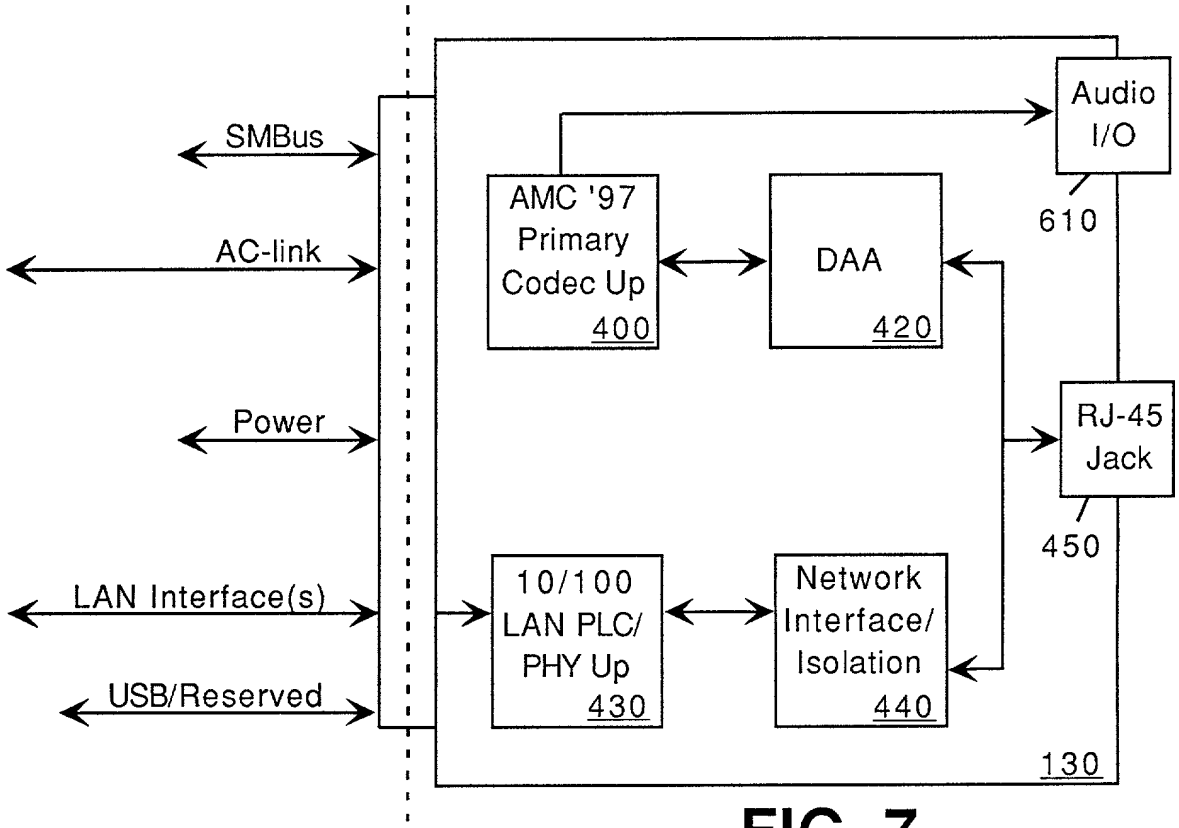
SMBus
AC-link
Power
LAN Interface(s)
USB/Reserved
AMC '97 Primary Codec Up 400
10/100 LAN PLC/ PHY Up 430
DAA 420
Network Interface/ Isolation 440
Audio I/O 610
RJ-45 Jack 450
130

FIG. 7

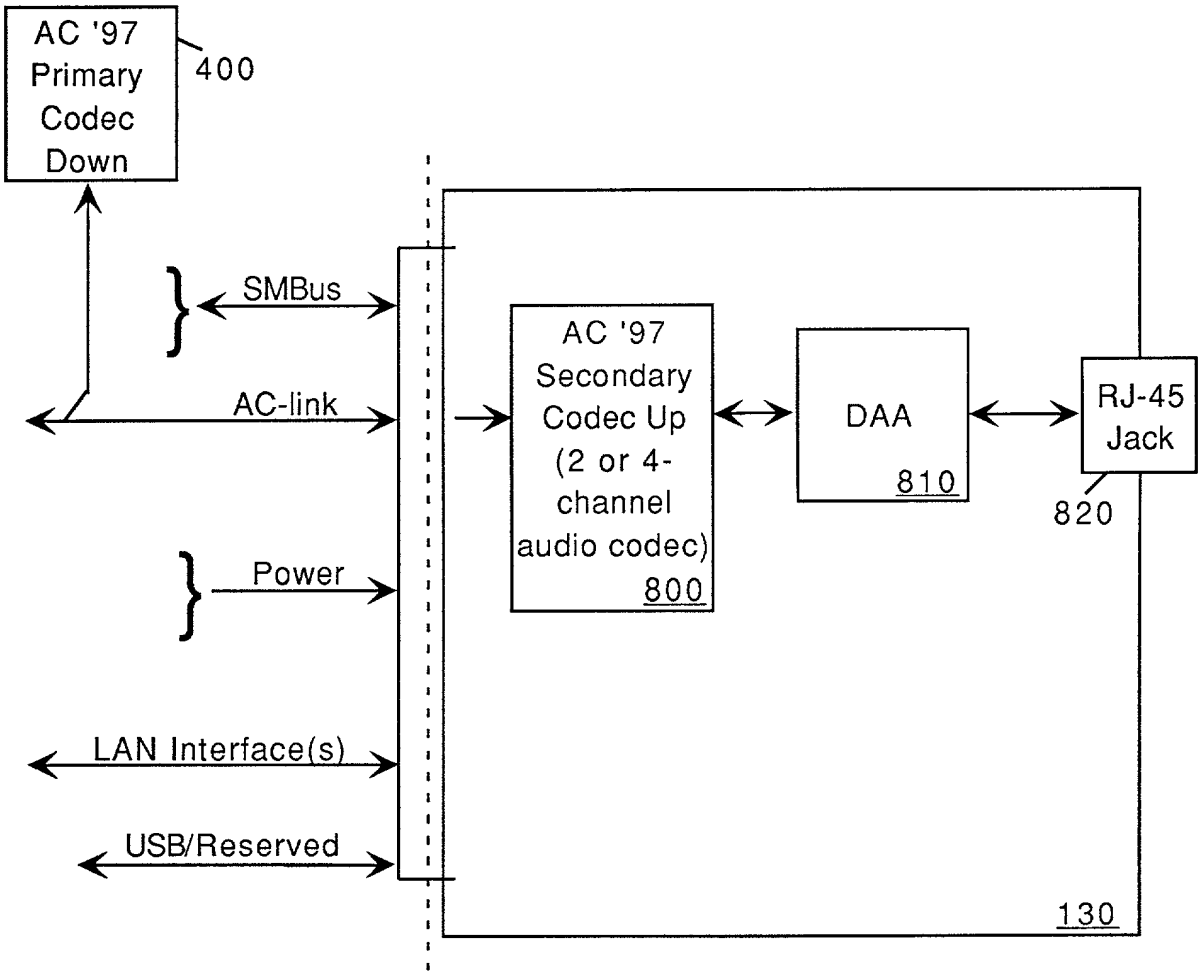
AC '97
Primary
Codec
Down
400
SMBus
AC-link
Power
LAN Interface(s)
USB/Reserved
AC '97
Secondary
Codec Up
(2 or 4-
channel
audio codec)
800
DAA
810
RJ-45
Jack
820
130

FIG. 8

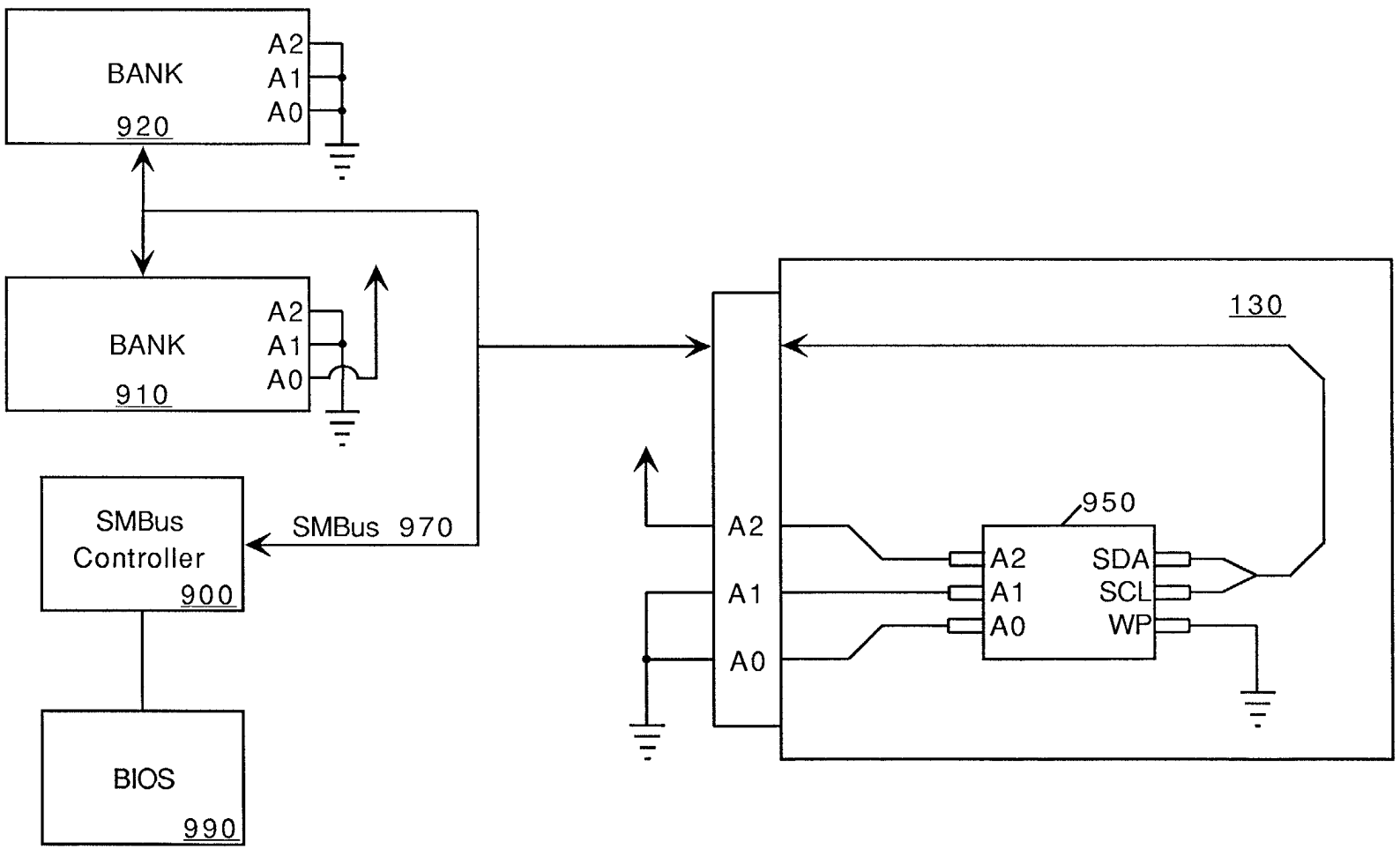
BANK
920
A2
A1
A0
BANK
910
A2
A1
A0
SMBus
Controller
900
SMBus 970
BIOS
990
130
950
A2
A1
A0
A2
A1
A0
SDA
SCL
WP

FIG. 9

Attorney's Docket No.: 042390.P8527 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MOTHERBOARD EXTENSION FEATURES TO PROVIDE PLUG AND PLAY INFORMATION

the specification of which

x is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

EL034434111US

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Paul A. Mendonsa **(Name of Attorney or Agent)**, **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** Paul A. Mendonsa **(Name of Attorney or Agent)**, **(503) 684-6200.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor **Brad A. Barmore**

Inventor's Signature _____ Date June 27, 2000

Residence Portland, OR USA (City, State) Citizenship USA (Country)

Post Office Address 18994 NW Astoria Drive
Portland, OR 97229

Full Name of Second/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Third/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

APPENDIX A

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Andrew C. Chen, Reg. No. 43,544; Thomas M. Coester, Reg. No. 39,637; Alin Corie, Reg. No. P46,244; Dennis M. deGuzman, Reg. No. 41,702; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Sanjeet Dutta, Reg. No. P46,145; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; Paramita Ghosh, Reg. No. 42,806; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Sang Hui Kim, Reg. No. 40,450; Eric T. King, Reg. No. 44,188; Erica W. Kuo, Reg. No. 42,775; Kurt P. Leyendecker, Reg. No. 42,799; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. 44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Daniel E. Ovanezian, Reg. No. 41,236; Marina Portnova, Reg. No. P45,750; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. P46,322; Thomas C. Webster, Reg. No. P46,154; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. 45,241; Steven D. Yates, Reg. No. 42,242; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Justin M. Dillon, Reg. No. 42,486; my patent agent, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; John N. Greaves, Reg. No. 40,362; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. 44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.